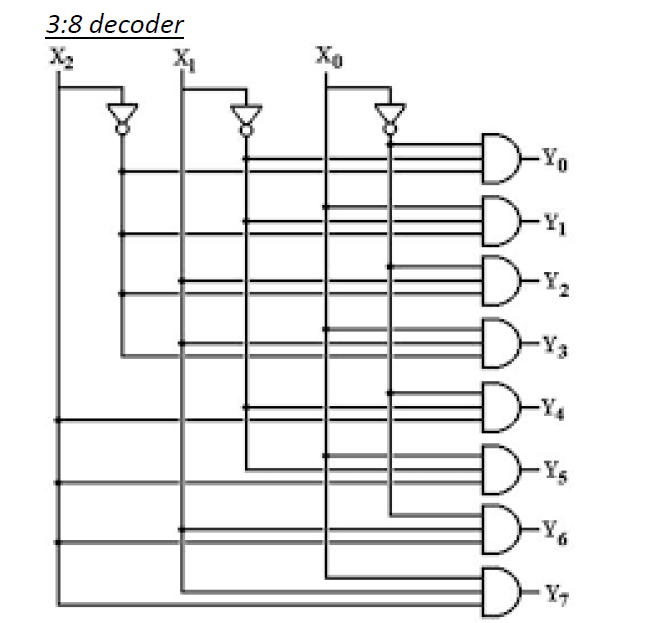
**Experiment 4**

**Aim-1: Implementation of 3:8 decoder using Behavioral Modelling in Verilog.**

**Software:** Xilinx Vivado Design Suite

**Theory:** Truth table of 8:1 Mux

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **IN2** | **IN1** | **IN0** | **OUT7** | **OUT6** | **OUT5** | **OUT4** | **OUT3** | **OUT2** | **OUT1** | **OUT0** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

****

**Procedure:**

1. Open the Xilinx Vivado Design Suite
2. Go to file and click new project
3. Enter the project name and click next
4. Select the family name of the FPGA Device, parameter setting and HDL is verilog click next and click finish.
5. Click new source.
6. Select Verilog module and type file name and click next.
7. Assign input and output port and click next.
8. Finally, the report is shown click finish.
9. Type the program save and check syntax error.
10. To see the output waveform select ISim simulator
11. Give values to the input variables using force clock or force constant and then click run
12. In wave window, click run icon and you can see corresponding output.
13. For synthesis of the design, open XST synthesis tool and run the design for synthesis.
14. Open RTL schematic and Technology schematic and understand implemented design on FPGA
15. Open synthesis result to know resource utilization of the design.

**Code:**

module decoder3to8\_ (

input [2:0] in,

output reg [7:0] out

);

always @(in)

case (in)

3'b000 : out = 8'b00000001;

3'b001 : out = 8'b00000010;

3'b010 : out = 8'b00000100;

3'b011 : out = 8'b00001000;

3'b100 : out = 8'b00010000;

3'b101 : out = 8'b00100000;

3'b110 : out = 8'b01000000;

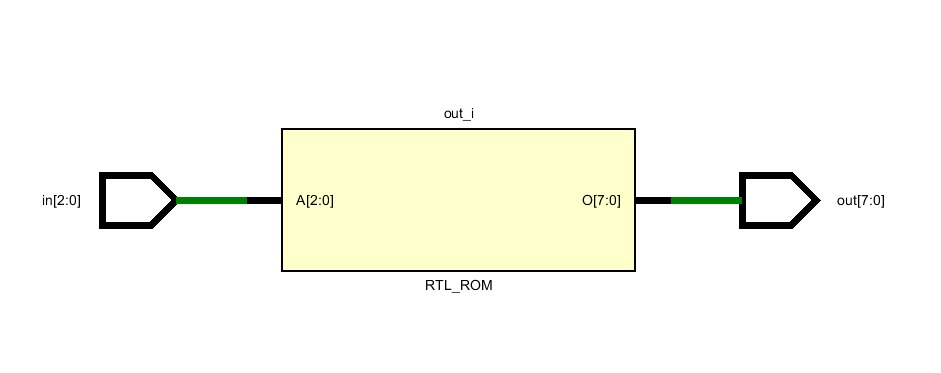
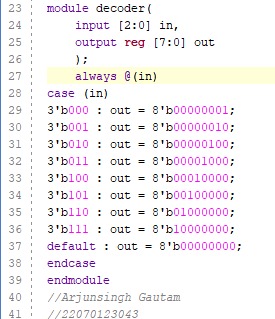
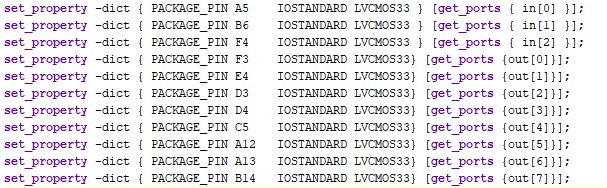
3'b111 : out = 8'b10000000;

default : out = 8'b00000000;

endcase

endmodule

**Result:**



Spartan-7 Physical Simulation

Constraint File

Verilog Code

Schematic Design

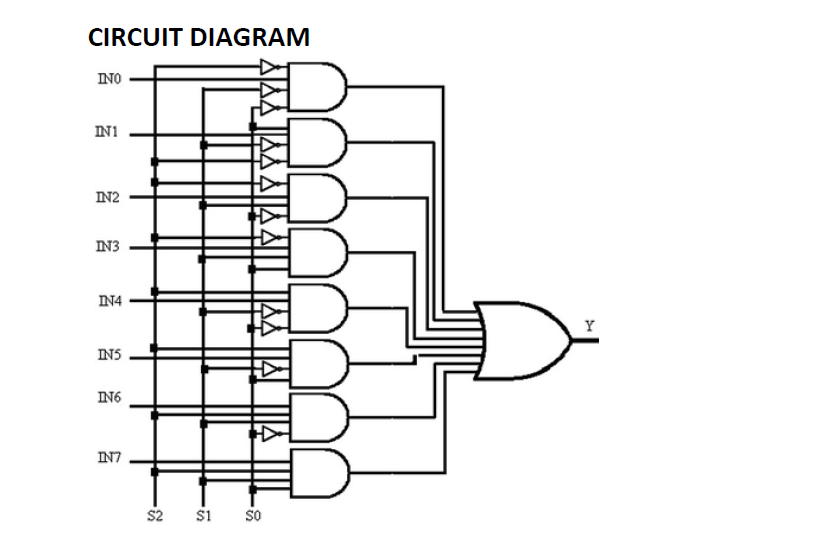
**Aim-2: Implementation of** 8**:1 mux using:**

1. **Dataflow modeling**
2. **Implementing the design of Spartan-7 kit**

**Apparatus:** Xilinx Vivado Design Suite

**Theory:** Truth table of 8:1 Mux

|  |  |  |  |
| --- | --- | --- | --- |
| **S2** | **S1** | **S0** | **Y** |
| 0 | 0 | 0 | I0 |
| 0 | 0 | 1 | I1 |
| 0 | 1 | 0 | I2 |
| 0 | 1 | 1 | I3 |
| 1 | 0 | 0 | I4 |
| 1 | 0 | 1 | I5 |
| 1 | 1 | 0 | I6 |
| 1 | 1 | 1 | I7 |



**Procedure:**

1. Open the Xilinx Vivado Design Suite
2. Go to file and click new project
3. Enter the project name and click next
4. Select the family name of the FPGA Device, parameter setting and HDL is verilog click next and click finish.
5. Click new source.
6. Select Verilog module and type file name and click next.
7. Assign input and output port and click next.
8. Finally, the report is shown click finish.
9. Type the program save and check syntax error.
10. To see the output waveform select ISim simulator
11. Give values to the input variables using force clock or force constant and then click run
12. In wave window, click run icon and you can see corresponding output.
13. For synthesis of the design, open XST synthesis tool and run the design for synthesis.
14. Open RTL schematic and Technology schematic and understand implemented design on FPGA
15. Open synthesis result to know resource utilization of the design.

**Code:**

**Dataflow Modelling**

module mux81\_dataflow(

input i0,i1,i2,i3,i4,i5,i6,i7,

input s0,s1,s2,

output out

);

assign out = s2?(s1?(s0?i7:i6):(s0?i5:i4)):(s1?(s0?i3:i2):(s0?i1:i0));

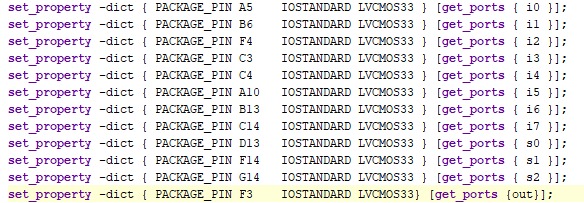
endmodule

**Result:**

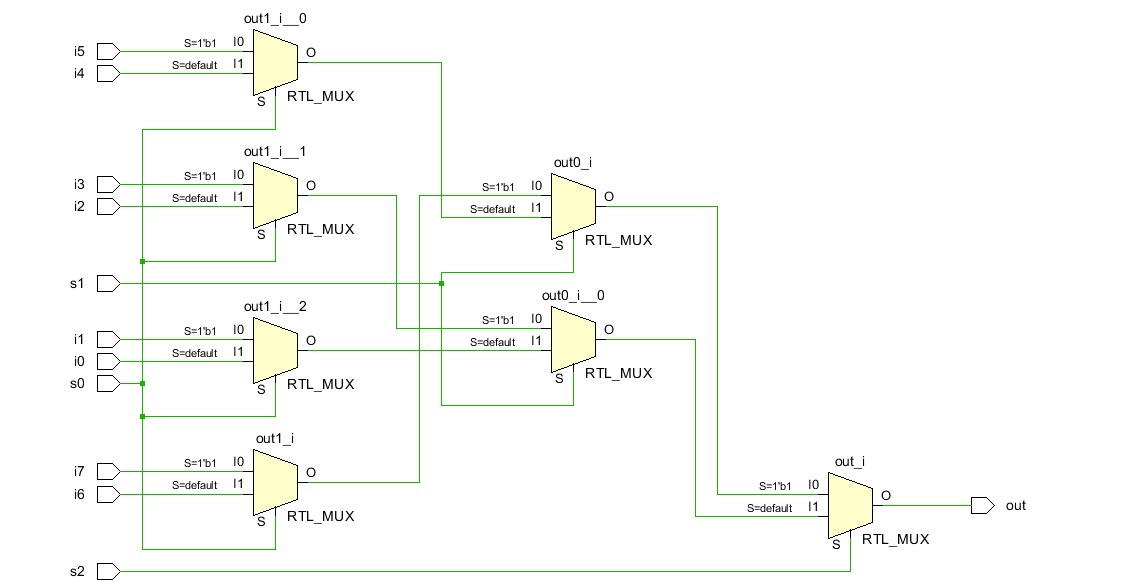
## 1.Verilog Code:



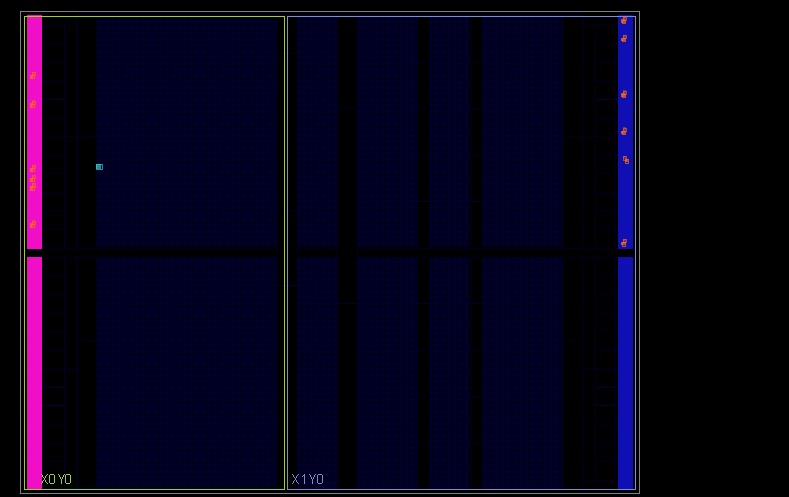
## 2.Constraint File:



## 3. Schematic Design:



## 4. Elaborate Design:



## 5.FPGA Kit Simulation:

**z**

**Conclusion:**

* In this experiment we study the functioning of a decoder and also implement the Verilog design on Spartan-7 Hardware board and physically stimulate the design
* We also study about multiplexer and implemented 8:1 multiplexer using data-flow level modelling on Spartan-7 FPGA kit